PCI based dual UART and printer port chip CH352

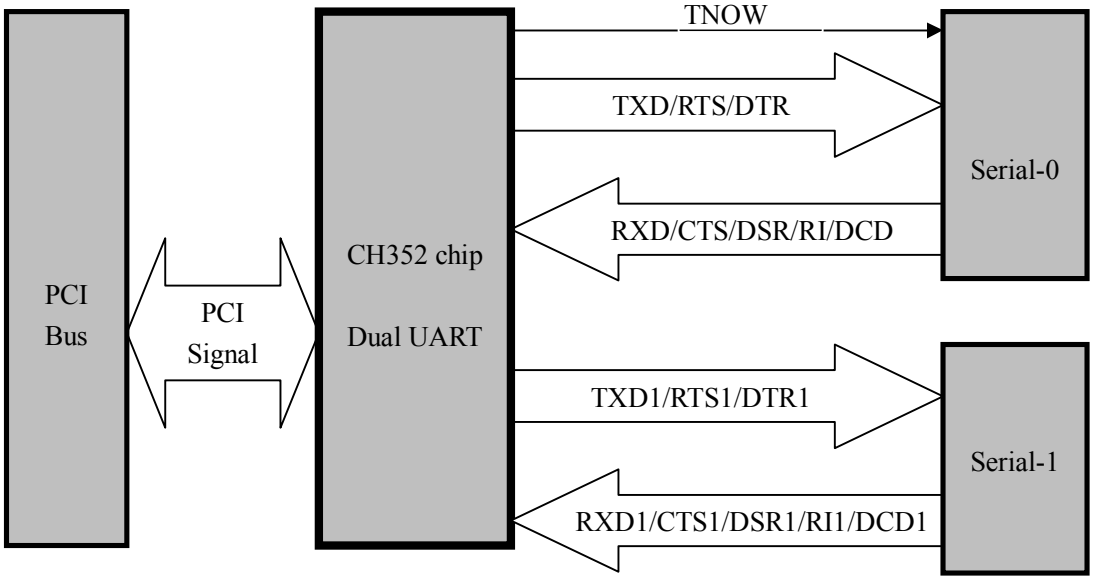
English DataSheet

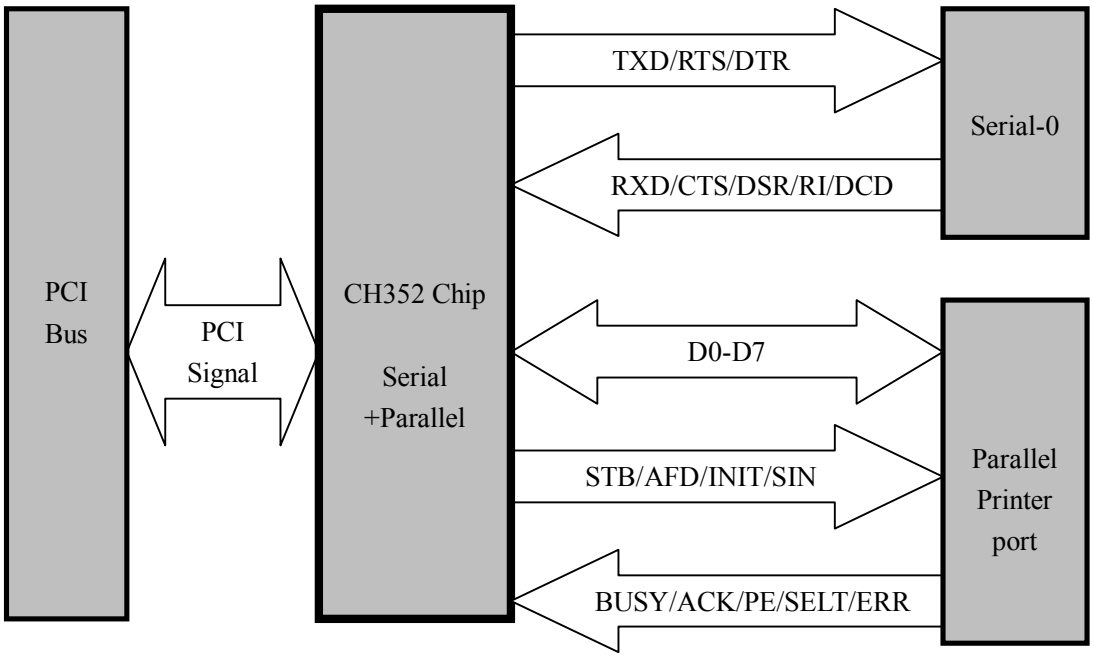
Version: 1A

http://wch.cn

1. Introduction

CH352 is a PCI based dual-channel high performance UART with EPP/ECP enhanced bi-directional parallel controller. It is compatible with 16C550. Adding one CH432Q, it can realize PCI bus based quadruple UART. UART supports semiduplex receive and transmit conversion automatic and IrDA infrared encode and decode, supporting communication baud rate up to 4Mbps, used for RS232 serial expansion, PCI high-speed serial with automatic hardware speed control, serial networking, RS485 communication, parallel interface/printer port expansion etc. The following image is application project.





2. Features

2.1. Introduction

● Can be configured as dual channel UART and parallel /printer port bus or quadruple channel UART based on PCI.

● Providing two wire serial host interface, hang serial EEPROM similar with 24C0X to store data which is not easy missing.

● Appointing Vendor ID, Device ID, Class Code and other information of PCI board in EEPROM.

● Drive supporting Windows 98/ME/2000/XP/Vista and Linux.

● 3.3V or 5V voltage, supporting serial low power sleep mode.

● Function is similar with CH365 adds CH432, providing dual UART, quadruple UART and eight serial application project.

● LQFP-100 lead-free, compatible with RoHS.

2.2. Serial interface

● Dual independence UART, compatible with 16C450, 16C550 and 16C552 with enhanced.

● Supporting 5,6,7,or 8 data bits and 1 or 2 stop bits.

● Odd, Even, No parity, space 0 and mark 1 etc

● Programmable Baud Rate, supporting 115200bps and up to 4Mbps baud rate.

● 16-byte FIFO buffer, supporting 4 FIFO trigger layers.

● Supporting MODEM signal CTS, DSR, RI, DCD, DTR, RTS, convert to RS232 level via 75232.

● Supporting CTS, RTS to realize auto handshake and auto transmit speed control, compatible with TL16C550C.

● Supporting serial frame error check, and Break circuit interval check.

● Supporting full duplex and semi-duplex serial communication, providing RTS transmit status signal to support RS485 receive and transmit automatic conversion.

● SIR infrared encode and decode, supporting 2400bps to 115200bps baud rate of IrDA communication.

● set clock oscillate internally, 22.1184MHz, 11.0592MHz or 7.3728MHzcrystal is optional.

2.3. Parallel

● Supporting such as SPP, Nibble, Byte, PS/2, EPP and ECP etc IEEE1284 parallel/printer port modes.

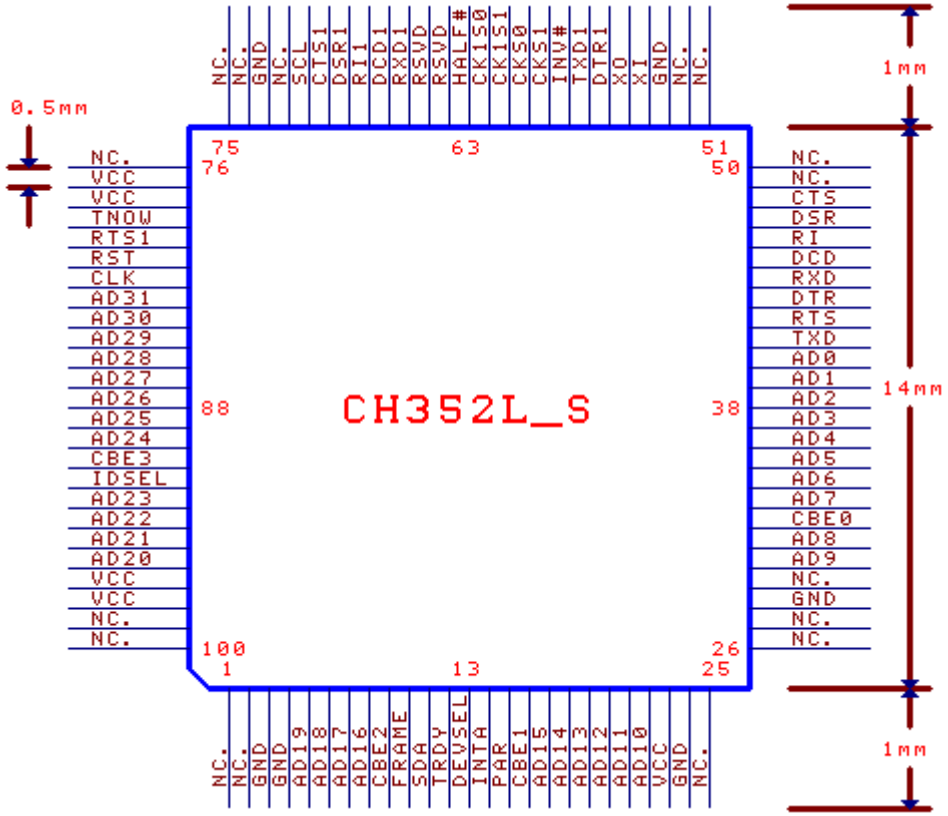
● Supporting bi-directional data transfer, the transfer speed is up to 2M Byte/S.

● With pull-up resistor which is needed by printer port, the peripheral circuit is easy.

● With 8255 mode 2, the parallel mode with hardware handshake function, used to connect with MCU bus to exchange data.

3. Package

dual serial



The detail application and pins of quadruple UART can refer to the second data sheet CH352DS2.PDF.

Package	Width of plastic	Pitch of pin		Instruction of package	Ordering type
LQFP-100	14mm x 14mm	0.5mm	19.7mil	Low profile quad flat package 100-pin	CH352L

4. Pins

4.1. Power wire

Pin NO.	Name	Type	Pin Description
23,77,78, 97,98	VCC	POWER	Positive Power
3,4,24, 28,53,73	GND	POWER	Public ground
64,65	RSVD	Reserved	Reserved pins, forbid to connect
1,2,25,26, 27,29,49, 50,51,52, 72,74,75, 76,99,100	NC.	NC.	Forbid to connect

4.2. PCI bus signal

Pin NO.	Name	Type	Pin Description
81	RST	IN	System reset signal, low active
82	CLK	IN	System clock signal, active with rising edge
83-90, 93-96, 5-8, 17-22, 30-31, 33-40	AD31～AD0	Tri-state output/input	Multiplex Address/Data Bus
91,9, 16,32	CBE3～CBE0	IN	Bus Command and Byte Enable
15	PAR	Tri-state bi-directional	Parity check wire
92	IDSEL	IN	Initialize device select wire, high active
10	FRAME	IN	Frame cycle start wire, low active
12	TRDY	Tri-state output	Target ready wire, low active
13	DEVSEL	Tri-state output	Target device select wire, low active
14	INTA	Drain open output	INTA interrupt request wire, low active

4.3. Serial interface 0 signal wire

Pin No.	Name	Type	Description
48	CTS	IN	MODEM signal, Clear-To-Send, low active, with feeble pull-up resistor
47	DSR	IN	MODEM signal, Data-Send-Ready, low active, with feeble pull-up resistor
46	RI	IN	MODEM signal, Ring-Indication, low active, with feeble pull-up resistor
45	DCD	IN	MODEM signal, Carrier-Detect, low active, with feeble pull-up resistor
44	RXD	IN	Asynchronous serial data input, with feeble pull-up resistor
43	DTR	OUT	MODEM signal, Data-Terminal-Ready, low active
42	RTS	OUT	MODEM signal, Request-Transmit, low active When semiduplex, serial data is transfer indication, high active
41	TXD	OUT	Asynchronous serial data output
79	TNOW	OUT	Serial data is transferring indication, high active

4.4. Serial interface 1 signal wire

Pin No.	Name	Type	Pin Description
70	CTS1	IN	MODEM signal, Clear-To-Send, low active, with feeble

			pull-up resistor
69	DSR1	IN	MODEM signal, Data-Send-Ready, low active, with feeble pull-up resistor
68	RI1	IN	MODEM signal, Ring-Indication, low active, with feeble pull-up resistor
67	DCD1	IN	MODEM signal, Carrier-Detect, low active, with feeble pull-up resistor
66	RXD1	IN	Asynchronous serial data input, with feeble pull-up resistor
56	DTR1	OUT	MODEM signal, Data-Terminal-Ready, low active
80	RTS1	OUT	MODEM signal, Request-Transmit, low active When semiduplex, serial data is transfer indication, high active
57	TXD1	OUT	Asynchronous serial data output

4.5. Assistant signal wire

Pin No.	Name	Type	Pin Description
54	XI	IN	Crystal oscillator input, connect with crystal and capacitance
55	XO	OUT	Crystal oscillator opposite output, connect with crystal and capacitance
60	CKS0	IN	Serial-0 internal benchmark clock frequency select port-0, with feeble pull-up resistor
59	CKS1	IN	Serial-0 internal benchmark clock frequency select port-1, with feeble pull-up resistor
62	CK1S0	IN	Serial-1 internal benchmark clock frequency select port-0, with feeble pull-up resistor
61	CK1S1	IN	Serial-1 internal benchmark clock frequency select port-1, with feeble pull-up resistor
63	HALF#	IN	Semiduplex communication enable, low active, with feeble pull-up resistor
58	INV#	IN	Serial opposite input mode enable, low active, with pull-up resistor
71	SCL	Drain open output input	Chip function configuration input, with pull-up resistor, connect with SCL pin of serial EEPROM configuration chip 24CXX
11	SDA	Drain open output input	External configuration chip enable, high active, with pull-down resistor Connect with SDA pin of EEPROM configuration 24CXX

5. Configuration

5.1. Global function configuration

CH352 has two main function modes: one is dual UART mode, the other is UART + parallel mode.

The SCL used to configure chip's function, and SDA used to enable external serial EEPROM configuration chip, consulting the following table.

SCL and SDA	SDA is suspended or connects with ground	SDA connects with pull-up resistor R2 to VCC
SCL is suspended	Serial-0+serial-1, no configuration	Serial-0+serial-1, enable external configure
SCL connects with ground or low-level	Serial-0+parallel, no configuration	Serial-0+parallel, no configuration
SCL connects with RST	Serial-0+parallel, no configuration	Forbid to use these setting, or the chip will be destroyed
SCL connects with R1 to RST	Serial-0+parallel, no configuration	Serial-0+parallel, enable external configure

In the table, the value of R1 is 2KΩ~3.3KΩ, and the value of R2 is 2KΩ~10KΩ.

5.2. External configure chip

If enable external configuration (SDA pull-up), CH352 will check the data in the external 24CXX configuration chip after every starting machine or PCI Bus reset. If the data is valid, automatically load to CH352 chip to replace PCI information.

The configure chip 24CXX has four pins or eight pins, and it is a serial EEPROM storage. Except supplying configuration information, it is also providing application program to protect other parameter. CH352 supports these types of 24CXX: 24C01(A),24C02,24C04,24C08,24C16 etc.

The following table is data define of 24CXX.

Byte Address	Short Name	Data Explanation	Default
01H-00H	VID	Vendor ID	Self define
03H-02H	DID	Device ID	Self define
04H	RID	Revision ID	Self define
07H-05H	CLS	Class Code	070002H
09H-08H	SVID	Subsystem Vendor ID	Self define
0BH-0AH	SID	Subsystem ID	Self define
0CH	CFG	External configuration chip valid token, bit7 must be 0, bit6 must be 1, bit0 is used to select internal frequency coefficient in serial + parallel mode	41H
1FH-0DH	RSVD	（Reserved unit）	00H 或 FFH
Other address	APP	Customer or application program self define unit	

5.3. Serial function configuration

In dual UART mode, the serial in CH352 supports full duplex or semiduplex communication. When HALF# connects with ground or low-level, CH352 will work in semiduplex mode. And the semiduplex communication has two applications: semiduplex serial (contains but not limited in RS485 communication application), IrDA infrared serial SIR. In semiduplex application, RTS pin (RTS1 in serial-1) is indicate that serial data is transferring, high active, used to automatic control RS485 transceiver transfer and receive switch. In infrared serial SIR application, RXD and TXD can directly connect with RXD and TXD in ZHX1810, HSDL3000, TFBS4711 and TFDU4100 infrared transceiver. The following is serial function configuration.

Pin status	HALF# is suspended or connects with high-level	HALF# connects with ground or low-level
CTS connects with high-level	Serial-0 is full duplex CTS used as MODEM signal	Serial-0 is infrared serial SIR
CTS connects with ground or low-level		Serial-0 is semiduplex, such as RS485
CTS1 connects with high-level	Serial-1 is full duplex CTS1 used as MODEM signal	Serial-1 is full duplex
CTS1 connects with ground or low-level		Serial-1 is semiduplex, such as RS485

5.4. Serial internal clock

CH352 has clock oscillator, connect one crystal between XI and XO, and two external capacitance connected from each side of XI and XO to GND. Then generate external clock signal for serial. Un-connect with crystal and capacitance, CH352 also input clock from external clock via XI pin.

CH352 can divide or multiply external clock signal which is from XI, and then generate internal benchmark clock for serial port 0 and 1. In order to compatible with 16C550 in current computer, the default value of internal clock is 1.8432MHz, and the baud rate is 115200bps. CH352 supports several clock frequencies. If the internal clock frequency is multiplied, and software has no change, the actual baud rate is also multiplied. For example, application software is set as 115200bps, the actual baud rate is 230400bps.

In dual UART mode, CKS0 and CKS1 in serial-0 can determine divide frequency or multiple frequency, change the external clock frequency to four internal clock frequency, and so that to support more serial baud rate. The following table is about CKS0/CKS1 and internal clock frequency generated by external crystal, the max serial baud rate. CK2X is bit5 in IER register of serial-1; CKS0/CKS1=1 means CKS0/CKS1 connects with high-level (or suspended), CKS0/CKS1=0 means CKS0/CKS1 connects with low-level (or connects with ground). Responds with serial-0, serial-1 frequency is determined by CK1S0 and CK1S1.

Register control bit Pin state	CK2X=0 and CKS0=1, CKS1=1	CK2X=0 and CKS0=0, CKS1=1	CK2X=0 and CKS0=1, CKS1=0	CK2X=1 or CKS0=0, CKS1=0
Internal frequency Coefficient	Divided by 12	Multiplied by 6	Divided by 4	Multiplied by 2
External crystal 22.1184MHz	1.8432MHz 115.2Kbps	3.6864MHz 230.4Kbps	5.5296MHz 345.6Kbps	44.2368MHz 2.7648Mbps
External crystal 11.0592MHz	0.9216MHz 57.6Kbps	1.8432MHz 115.2Kbps	2.7648MHz 172.8Kbps	22.1184MHz 1.3824Mbps
External crystal 7.3728MHz		1.2288MHz 76.8Kbps	1.8432MHz 115.2Kbps	14.7456MHz 921.6Kbps
External crystal 0.9216MHz				1.8432MHz 115.2Kbps
External crystal 32MHz				64MHz 4Mbps
External crystal 18.432MHz				36.864MHz 2.304Mbps
External crystal 14.7456MHz				29.4912MHz 1.8432Mbps

6. Register

6.1. Basic declare

6.1.1. Attribute abbreviations: R=Read Only, W=Read and Write, S=Read only but can be set in advance, ….=suspension points

6.1.2. Number: H indicates hex, or binary system.

6.1.3. Value wildcard and attribute: r=Reserved (forbid to use), X=Any, ….=suspension points

6.2. PCI configuration space

Type	Address	Register Name	Register Attribute	Default value after reset
Standard PCI Device Configure spare	01H-00H	VID: Vendor ID	SSSS	4348H
	03H-02H	DID: Device ID	SSSS	3253H or 5053H, see the following
	05H-04H	Command register: Command	RRRRRRRRRRRRRRRW	0000000000000000
	07H-06H	Status register: Status	RRRRRRRRRRRRRRRR	000000100000x000
	08H	Revision ID	SS	10H
	0BH-09H	Class Code	SSSSSS	070002H
	0FH-0CH		RRRRRRRR	00000000H
	13H-10H	Serial-0: I/O Base Address 0	WWWWWWWWWWWWWWWW WWWWWWWWWWWWWRRR	0000000000000000 0000000000000001
	17H-14H	Serial-1 or parallel: I/O Base Address 1	WWWWWWWWWWWWWWWW WWWWWWWWWWWWWRRR	0000000000000000 0000000000000001
	2BH-18H		RRRR….RRRR	0000….0000H
	2FH-2CH	Subsystem ID	SSSSSSSS	Same with DID+VID
	3BH-30H		RRRR….RRRR	0000….0000H
	3FH-3CH	Interrupt Line & Pin	RRRRRRRRRRRRRRRR RRRRRRRRWWWWWWWW	0000000000000000 0000000100000000
Configure register	40H	Configure control register CFG_CTRL	RRRRRRWW	x0xx0011
	41H	Configure status register CFG_STAT	RRRRRRRR	x000000x
	7FH-42H	Reserved	（Forbid to use）	（Forbid to use）

The DID in configuration spare, is3253H in dual UART mode. It is 5053H in UART+ Parallel mode.

6.3. Bits of configuration register

Register Name	Address	Attribute	Explanation of bits	Bit value=0	Bit value=1
Configure control register CFG_CTRL （configure spare 40H address）	Bit-0	W	Set SDA pin output value	Low	High
	Bit-1	W	Set output value of SCL pin	Low	High
	Bit-4	R	Input status of SDA pin	Low	High
	Bit-5	R	Input status of SCL	Low	High

	Bit-7	S	24CXX configure chip enable status	Forbid to use	Start
Configure status register CFG_STAT （configure spare 41H address）	Bit-0	S	Configure chip valid token CFG bit-0	Bit-0=0	Bit-0=1
	Bit-7	S	24CXX configure data valid	Invalid	valid

6.4. Serial port register

The serial ports of CH352 are comply with industrial standard 16550 and enhanced. In the table with gray is enhanced function, except these, other register can consult single serial port chip 16C550 or dual serial ports CH432.The real address of serial port 0 register is I/O base address 0 adds offset address in the table, and the real address of serial port 1 register is I/O base address 1 adds offset address. Except SLP/CK2X register, the registers of serial port 0 is the same with serial port 1. The DLAB is bit-7 of register LCR, X indicates taking no care of DLAB value, R0 indicates the register is Read Only, W0 indicates the register is Write Only, R/W indicates register Read-and-Write.

Add.	DLAB	R/W	Name	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	RO	RBR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	0	WO	THR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	0	R/W	IER	RESET	LOWPOWER	SLP/CK2X	0	IEMODEM	IELINES	IETHRE	IERECV
2	X	RO	IIR	FIFOENS	FIFOENS	0	0	IID3	IID2	IID1	NOINT
2	X	WO	FCR	RECVTG1	RECVTG0	0	0	0	TFIFORST	RFIFORST	FIFOEN
3	X	R/W	LCR	DLAB	BREAKEN	PARMODE1	PARMODE0	PAREN	STOPBIT	WORDSZ1	WORDSZ0
4	X	R/W	MCR	0	0	AFE	LOOP	OUT2	OUT1	RTS	DTR
5	X	RO	LSR	RFIFOERR	TEMT	THRE	BREAKINT	FRAMEERR	PARERR	OVERR	DATARDY
6	X	RO	MSR	DCD	RI	DSR	CTS	△DCD	△RI	△DSR	△CTS
7	X	R/W	SCR	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	1	R/W	DLL	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
1	1	R/W	DLM	Bit-15	Bit-14	Bit-13	Bit-12	Bit-11	Bit-10	Bit-9	Bit-8

The following table is registers' default value after power-on reset or PCI bus reset or serial port software reset.

Register Name	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
IER	0	0	0	0	0	0	0	0
IIR	0	0	0	0	0	0	0	1
FCR	0	0	0	0	0	0	0	0
LCR	0	0	0	0	0	0	0	0
MCR	0	0	0	0	0	0	0	0
LSR	0	1	1	0	0	0	0	0
MSR	DCD	RI	DSR	CTS	0	0	0	0
SCR	hold	hold	hold	hold	hold	hold	hold	hold
FIFO	Reset, contain transferring FIFO and receiving FIFO							
TSR	Reset, TSR is serial port shift register							
RSR	Reset, RSR is serial port receive shift register							
Other	Undefined							

RBR: Receive Buffer Register, if DATARDY of LSR is 1, then can read received data from this register. If FIFPEN is 1, data received from RSR will be store in FIFO first, then be read from this register.
THR: Transfer Hold Register, contains transferring FIFO, used to write data which will be transfer. If FIFO is 1, then data which will be written will be store in transfer FIFO first, then output one by one from TSR.
IER: Interrupt enable register, contains enhanced function control bit and serial port interrupt enable.

RESET: If the bit is 1, then software reset serial port. This bit can automatically be cleared, doesn't need software to clear.

LOWPOWER: When the bit is 1, close internal benchmark clock of serial port to set into low-power status.

SLP/CK2X: This bit in serial port 0 and 1 is different, serial port 0 is SLP, when it is 1, close clock oscillator, so serial port 0 and 1 step into sleep status. Serial port 1 is CK2X, when it is 1, multiply 2 of the external clock signal and then as internal benchmark clock of serial port 0 and 1. Don't controlled by CKS0, CKS1, CK1S0, CK1S1

IEMODEM: When this bit is 1, allow interrupt when Modem input status has changed.

IELINES: When this bit is 1, allow interrupt of receive wire status.

IETHRE: when this bit is 1, allow transfer keep register blank interrupt.

IERECV: When this bit is 1, allow interrupt when receiving data.

IIR: Interrupt identify register, used to analyse interrupt source and deal with it.

FIFOENS: FIFO start status, when it is 1, indicates starting FIFO.

Bits of IIR register				priority	Interrupt type	Interrupt source	Method of clear interrupt
IID3	IID2	IID1	NOINT				
0	0	0	1	No	No interrupt	No interrupt	
0	1	1	0	1	Receive wire status	OVERR、PARERR、FRAMEERR、BREAKINT	Read LSR
0	1	0	0	2	Receive data valid	Number of received bytes up to FIFO spring	Read RBR
1	1	0	0	2	Receive data over time	Over four data time but don't receive the next data	Read RBR
0	0	1	0	3	THR empty	Transfer hold register is empty, IETHRE change from 0 to , and enable interrupt newly	Read IIR Or write THR
0	0	0	0	4	MODEM input has change	△CTS、△DSR、△RI、△DCD	Read MSR

FCR: FIFO-Control-Register used to enable and reset FIFO.

RECVTG1 and RECVTG0: Set receiving interrupt of FIFO and spring of hardware flow control, 00 corresponding to one byte, receives one byte and generates usable interrupt, enable hardware flow control and invalid RTS pin, 01 corresponding 4 bytes, 10 corresponding 8 bytes, 11 corresponding 14 bytes.

TFIFORST: When this bit is 1, clear data in transfer FIFO (don't contain TSR), this bit can auto clear as 0, don't need software.

RFIFORST: When this bit is 1, clear data in receive FIFO (don't contain RSR), this bit can auto clear as 0, don't need software.

FIFOEN: When this bit is 1 start FIFO, when this bit is 0 forbid FIFO, after forbid FIFO it is 16C450 compatible mode, indicates FIFO only one byte.

LCR: Line-Control-Register used to control format of serial ports communication.

DLAB: this bit is divisor flip-latch store enable, when it is 1,store DLL and DLM; when it is 0, store RBR/THR/IER.

BREAKEN: When this bit is 1, enforce to generate BREAK line interval.

PARMODE1 and PARMODE0: When PAREN is 1, set frame of parity check bit: 00 is Odd, 01 is Even, 10 is mark bit (MARK is 1), 11 is space bit (SPACE, clear as 0).

PAREN: When this bit is 1, allow generating parity check bit when transfer and check parity when receive; when this bit is 0, no parity check bit.

STOPBIT: When this bit is 1, has two stop bits; when this bit is 0, has one stop bit.

WORDSZ1 and WORDSZ0: Set word length, 00-5 data bits, 01-6 data bits, 10-7 data bits, 11-8 data bits

MCR: MODEM control register, used to control MODEM output.

AFE: When this bit is 1, allow CTS and RTS hardware auto flow control., If AFE is 1, only transfer the next data after checking CTS input is valid (low active),or pause serial port transfer. When AFE is 1, CTS input status has change, but don't generate MODEM status interrupt. If AFE is 1 and RTS is 1, when receive FIFO is empty, serial port will automatically valid RTS pin (low-level active). When received bytes up to spring, serial ports will automatically invalid RTS pin and valid RTS pin when receive FIFO is empty. Using hardware auto control, connecting the second part CTS pin with RTS pin, and transfer the second RTS pin to CTS pin. Use hardware auto flow control, connect CTS in the second party to RTS in the other party, and connect RTS in the second party to CTS in the other party.

LOOP: when this bit is 1, enable internal loop test mode. In this mode, all serial output pin are invalid, TXD inner return to RXD (TSR output inner return to RSR input), RTS inner return to CTS, DTR inner return to DSR, OUT1 inner return to R1, OUT2 inner return to DCD.

OUT2: when this bit is 1, allow interrupt request output at serial, or serial don't generate actual interrupt request.

OUT1: this bit is user self-define MODEM control, un-connect to output pin.

RTS: when this bit is 1, RTS pin output is valid (low active), or RTS output invalid.

DTR: when this bit is 1, DTR pin output is valid (low active), or DTR output invalid.

LSR: line status register, used to query mode analyse serial status.

RFIFOERR: when this bit is 1, indicates there is one PARERR, PRAMEERR or BREAKINT error at least in receive FIFO.

TEMT: when this bit is 1, indicates transfer keep register THR and transfer shift register TSR are empty.

THER: when this bit is 1, indicates transfer keep register THR is empty.

BREAKINT: when this bit is 1, indicates checking BREAK line interval.

FRAMEERR: when this bit is 1, data frame error reads from receive FIFO, lack of valid stop bit.

PARERR: when this bit is 1, data parity error reads from receive FIFO.

OVERR: when this bit is 1, indicates receive FIFO buffer is over.

DATARDY: when this bit is 1, indicates receive FIFO has received data, after reading all data in FIFO, this bit can be clear automatically.

MSR: MODEM status register, used to query MODEM status.

DCD: this bit is opposite of DCD pin, when it is 1, indicates DCD pin is valid (low-level active).

RI: this bit is opposite of RI pin, when it is 1, indicates RI pin is valid (low-level active).

DSR: this bit is opposite of DSR, when it is 1, indicates DSR pin is valid (low-level active).

CTS: this bit is opposite of CTS, when it is 1, indicates CTS pin is valid (low-level active).

△DCD: this bit is 1, indicates DCD pin input status has changed.

△RI: this bit is 1, indicates RI pin input status has changed.

△DSR: this bit is 1, indicates DSR pin input status has changed.

△CTS: this bit is 1, indicates CTS pin input status has changed.

SCR: user can define register by self.

DLL and DLW: baud rate divisor flip-latch, DLL is low byte, DLW is high byte, and the 16 bits data composed of DLL and DLW is used for serial baud rate generator. Divisor=serial internal benchmark clock/16/the needed communication baud rate. If serial internal benchmark clock is 1.8432MHz, the needed communication baud rate is 9600bps, then the dicisor=1843200/16/9600=12.

7. Function

7.1. Query and interrupt

The dual UART shares one PCI interrupt query pin in CH352. After entering PCI interrupt service, analyse whether CH352 query interrupt, and which serial is interrupting. When entering interrupt service, read the IIR register in serial-0 first, and if there is interrupt, deal with it and then quit. If there is no interrupt, read IIR register in serial-1, if there is interrupt, deal with it then quit. If there is no interrupt, quit directly. When the serial has affirmed, analyse LSR register if necessary, analyse interrupt reason and deal with it.

If serial works on interrupt mode, set IER register to allow relative interrupt query, and set OUT2 in MCR register to allow output interrupt.

If serial works on query mode, un-set IER and OUT2 in MCR, query LSR register and deal with it.

7.2. Serial transaction

The detail information can consult serial 16C550 or dual UART CH432.

7.3. Application

The serial output pins are CMOS level in CH352, compatible with TTL level. The input pins are compatible with CMOS level and TTL level, convert to RS232 serial via RS232 level conversion.

In order to work, the serial of CH352 needs the external to provide clock signal for XI. In common, clock signal is generated by inverter in CH352 through oscillating of crystal keeping frequency. After power-on reset or PCI bus reset, the bit-0 of PCI configuration spare command register is 0 (forbid I/O spare), CH352 automatically close clock oscillating, so the serial 0 and serial 1 step into sleep mode. Until CH352 is assigned I/O base address and the bit-0 of command register is 1, the clock oscillating is started.

In UART, CH352 contains these pins: data transfer pins and MODEM liaison signal pins. Data transfer pins contain: TXD and RXD, high-level in default. MODEM liaison signal contain: CTS, DSR, RI, DCD, DTR, RTS, high-level in default. All the MODEM liaison signal pins can be I/O pins, controlled by computer application program.

CH352 sets absolute transceiver buffer and FIFO, supporting simplex, semiduplex or full duplex asynchronism serial communication. Serial data contain one low-level starting bit, 8 data bits, 0 or one check bit or token bit, 1 or 2 high-level stop bit, supporting odd/even/token/blank. CH352 supports the communication baud rate: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M and so on. Band rate error of serial transmit signal is less than 0.2%, the allowance band rate error of serial receive signal is no less than 2%.

In Windows and Linux OS, the drive of CH352 is compatible with standard serial, so the most former serial application programs are compatible, no need to modify.

CH352 can be used to expand the extra high speed RS232 serial, high baud rate serial which supports auto hardware speed control, RS422 or RS485 communication interface, SIR infrared communication interface etc. via PCI bus.

8. Parameter

8.1. Absolute maximum rating (Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions can affect device operation and reliability.)

Name	Parameter note		Min.	Max.	Units
TA	Operation temperature	VCC=5V	-40	85	℃
		VCC=3.3V	-40	65	
TS	Storage temperature		-55	125	℃
VCC	Source Voltage（VCC connects to power, GND connects to ground）		-0.5	6.0	V
VIO	Voltage at input or output pin		-0.5	VCC+0.5	V

8.2. Electrical parameter (test conditions: TA=25℃,VCC=5V,exclude pin connection of PCI bus)
(The every current parameter must multiply the coefficient of 40% when the power is 3.3V)

Name	Parameter note	Min.	Typical	Max.	Units
VCC	Supply voltage（consult the following note）	3.3	5	5.3	V
ICC	Operate current	1	15	50	mA
VIL	Input voltage (LOW)	-0.5		0.8	V
VIH	Input voltage(HIGH)	2.0		VCC+0.5	V
VOL	Output voltage LOW（4mA draw current）			0.5	V
VOH	Output voltage HIGH（2mA output current）	VCC-0.5			V
IIN	Input current at input pin without pull-up resistor			10	uA
IUP1	Input current at input pin with feeble pull-up resistor	3	5	170	uA
IUP2	Input current at input pin with pull-up resistor	18	30	200	uA
IUPscl	Pull-up input current in SCL pin	150	250	400	uA
IDN	Input current in input pin with pull-down resistor	-18	-30	-80	uA

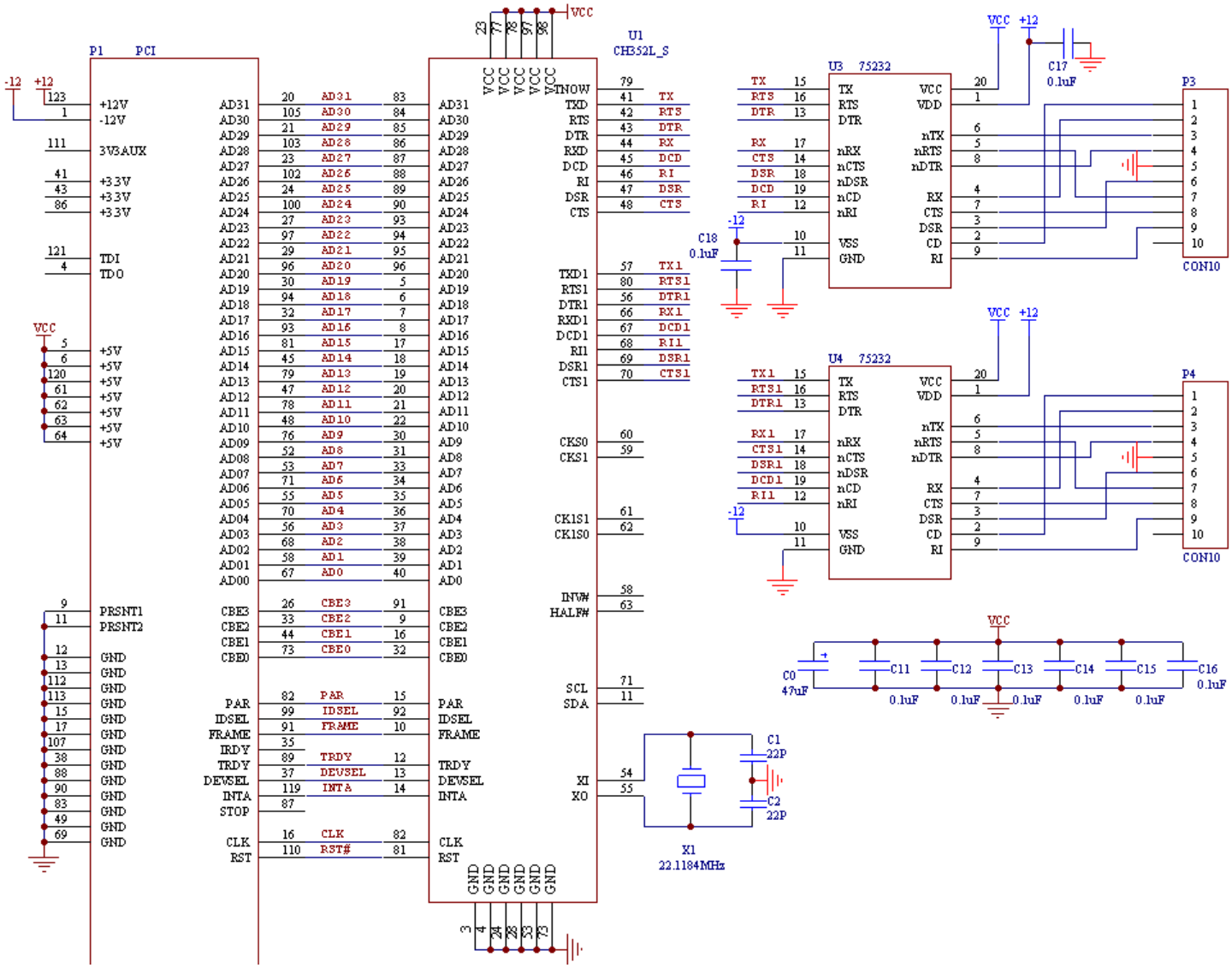
Note: The input endurance voltage is source voltage adds 0.5V of CH352. For example, when CH352 works in 3.3V, the outside providing voltage can't pass 3.8V. When the source voltage of CH352 is lower than 4V, the host frequency of PCI bus is no pass 33MHz, as PCI bus can't work at above 33MHz.

8.3. Time sequence parameter (test conditions: TA=25℃, VCC=5V, FCLK=33.3MHz, refer the following picture)

Name	Parameter note	Min.	Typical	Max.	Units
FCLK	CLK input frequency（PCI bus host frequency）	0	33.3	40	MHz
FSCL	SCL output frequency when auto load（2-wire interface host frequency）	FCLK / 128 = 260			KHz
FXI	XI input frequency, crystal frequency	0.9216	22.1184	32	MHz

9. Application

9.1. Dual RS232 UART (following image)

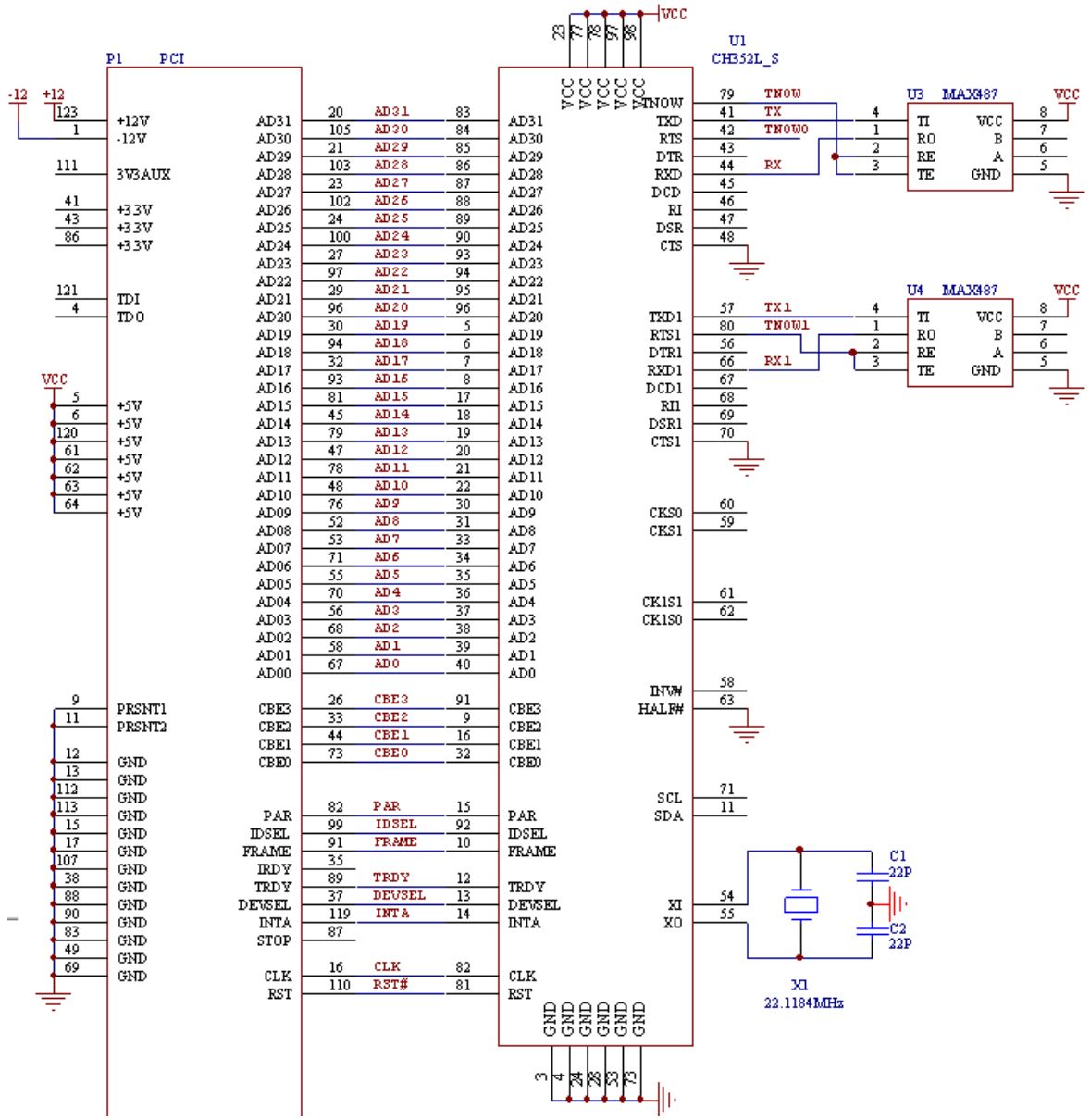


This is PCI dual channels UART circuit based on CH352 chip. U3 and U4 are RS232 level convert chip 75232, P3 and P4 are 10 pins two lines needles or DB9 needles. X1 and X2 are used for clock oscillator circuit. C0 and C11~C18 are used to power decoupling. C11~C18 are 0.1uF capacitances, they are made of monolithic or high frequency ceramic, connect next to four power pin in CH352 or 75232 chip.

CH352 is high frequency numeric circuit, pay attention on signal impedance matching, consult PCI criterion when designing PCB board. The PCI signal wire is less than 35mm in CH352, adapt arc wire or 45 degree wire, avoid right-angle or acute angle wire. Lay the signal wire in elements side, spare the other side to connect with ground. The length of CLK is between 50mm~65mm, it isn't near with other signal wire. Recommend to connect with ground or cover copper beside CLK and or the other side PCB board, decrease the disturber by other signal wires.

9.2. Dual RS485 interface (following image)

This is PCI dual RS485 interface circuit based on CH352, U3 and U4 is transceiver chip.



9.3. Connect configuration chip (following image)

The following is CH352 connect with external configuration chip 24C02, R2 is used to SDA pull up.