PCI based dual UART and printer port chip CH352

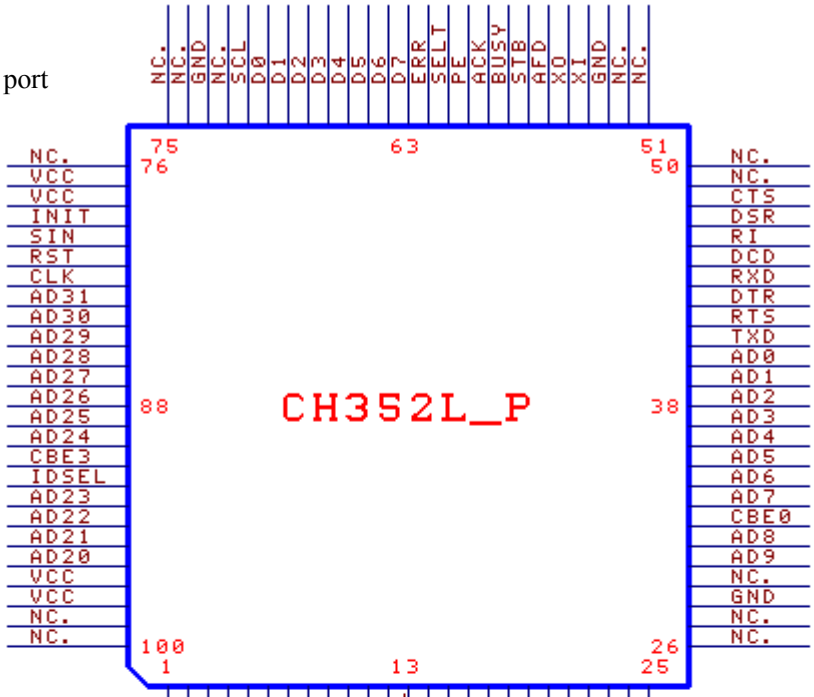
the second DataSheet: UART+parallel

Version: 1A

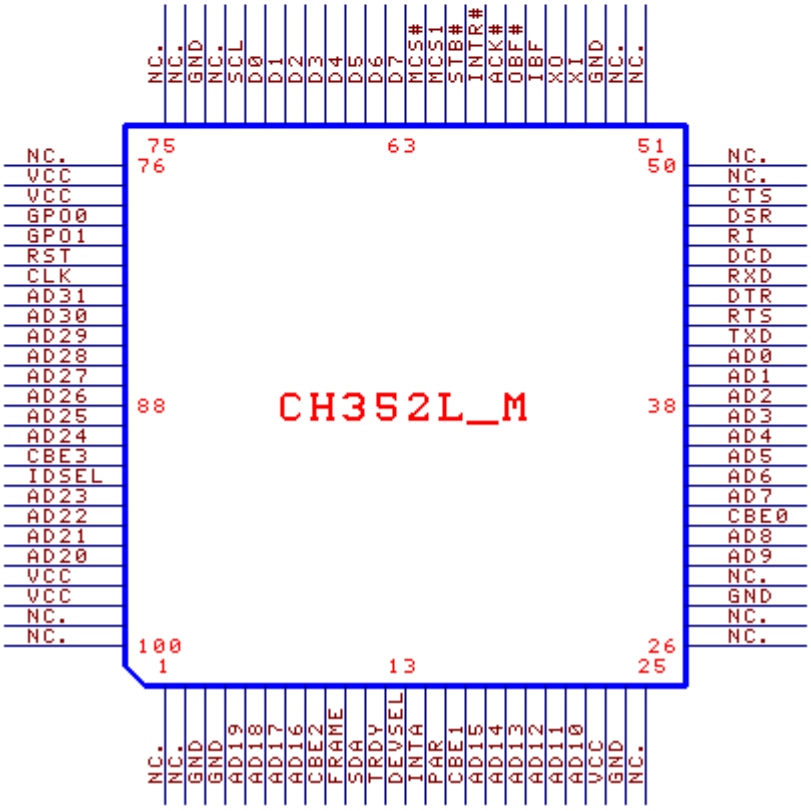
http://wch.cn

1. Package

UART+parallel/printer port



UART+8255 parallel



The information about dual UART and pins image can consult the first DataSheet CH352DS1.PDF.

2. Pins

2.1. Power wires

Pin No.	Name	Type	Pin Description
23,77,78, 97,98	VCC	POWER	Positive Power
3,4,24, 28,53,73	GND	POWER	Public ground
1,2,25,26, 27,29,49, 50,51,52, 72,74,75, 76,99,100	NC.	NC.	Forbid to connect

2.2. PCI bus signal

Pin NO.	Name	Type	Pin Description
81	RST	IN	System reset signal, low active
82	CLK	IN	System clock signal, active with rising edge
83-90, 93-96, 5-8, 17-22, 30-31, 33-40	AD31～AD0	Tri-state output/input	Multiplex Address/Data Bus
91,9, 16,32	CBE3～CBE0	IN	Bus Command and Byte Enable
15	PAR	Tri-state bi-directional	Parity check wire
92	IDSEL	IN	Initialize device select wire, high active
10	FRAME	IN	Frame cycle start wire, low active
12	TRDY	Tri-state output	Target ready wire, low active
13	DEVSEL	Tri-state output	Target device select wire, low active
14	INTA	Drain open output	INTA interrupt request wire, low active

2.3. Serial interface 0 signal wires

Pin No.	Name	Type	Description
48	CTS	IN	MODEM signal, Clear-To-Send, low active, with feeble pull-up resistor
47	DSR	IN	MODEM signal, Data-Send-Ready, low active, with feeble pull-up resistor
46	RI	IN	MODEM signal, Ring-Indication, low active, with feeble pull-up resistor
45	DCD	IN	MODEM signal, Carrier-Detect, low active, with feeble pull-up resistor
44	RXD	IN	Asynchronous serial data input, with feeble pull-up resistor
43	DTR	OUT	MODEM signal, Data-Terminal-Ready, low active
42	RTS	OUT	MODEM signal, Request-Transmit, low active When semiduplex, serial data is transfer indication, high active
41	TXD	OUT	Asynchronous serial data output

2.4. Printer port signal wires

Pin No.	Name	Type	Description
63-70	D7～D0	Tri-state Bi-directional	8-bit parallel data output and input, with pull-up resistor, connect with DATA7~DATA0
57	STB	OUT	Data strobe output, low active, connect with STROBE
56	AFD	OUT	Auto Feed output, low active, connect with AUTO-FEED
79	INIT	OUT	Initialize printer, low active, connect with INIT
80	SIN	OUT	Select printer, low active, connect with SELECT-IN

62	ERR	IN	Printer Data Error, low active, with strong pull-up resistor, connect with ERROR or FAULT
61	SLCT	IN	Printer selected, high active, with strong pull-up resistor, connect with SELECT or SLCT
60	PE	IN	Paper Empty, high active, with strong pull-up resistor, connect with PEMPTY or PERROR
59	ACK	IN	Printer data Acknowledge, rising edge active, with strong pull-up resistor, connect with ACK
58	BUSY	IN	Printer Busy, high active, with strong pull-up resistor connect with BUSY

2.5. 8255 parallel signal wires

The following 8255 parallel signal wires is about re-define of printer port signal wires.

Pin No.	Name	Type	Description
63-70	D7～D0	Tri-state Bi-directional	8-bit parallel data tri-state output and input, with pull-up resistor
57	OBF#	OUT	Download buffer full state output, low active, used for query
58	ACK#	In	Download data read pulse input, low active, with strong pull-up resistor
56	IBF	OUT	Upload buffer full state output, high active, used for query
60	STB#	IN	Upload data write pulse input, low active, with strong pull-up resistor
62	MCS#	IN	Parallel chip select input, low active, with strong pull-up resistor, connect with address encode
61	MCS1	IN	Parallel chip select input, high active, with strong pull-up resistor, connect with address encode
59	INTR#	IN	PCI interrupt query input, rising edge active, with strong pull-up resistor
79	GPO0	OUT	Output pin, low-level in default
80	GPO1	OUT	Output pin, high-level in default

2.6. Assistant signal wires

Pin No.	Name	Type	Description
54	XI	IN	Crystal oscillator input, connect with crystal and capacitance
55	XO	OUT	Crystal oscillator opposite output, connect with crystal and capacitance
71	SCL	Drain open output and input	Chip function configuration input, with pull-up resistor, can connect with EEPROM configuration chip24CXX SCL pin
11	SDA	Drain open output and input	External configuration chip enable, high active, with pull-down resistor, can connect with EEPROM configuration chip 24CXX SDA pin

3. Configuration

CH352 has two function modes: dual UART mode and UART+parallel mode. The detail information about function configuration method, external configuration chip, and the serial internal clock can consult the first DataSheet.

In UART+parallel mode, the serial-0 can be divided or multiplied by SCL pin in CH352. Change the external clock frequency to two internal clock frequencies, so it can support more serial baud rate. The following table is internal clock frequency and max serial baud rate generated by SCL pin and external crystal. The CFG is the token of external configuration chip is valid.

Pin state	SCL connects with ground or low-level	SCL connects with RST	SCL connects with R1 to RST	
			CFG bit-0 is 1	CFG bit-0 is 0
Internal frequency Coefficient	Divided by 12	Multiplied by 2	Divided by 12	Multiplied by 2
External crystal 22.1184MHz	1.8432MHz 115.2Kbps	44.2368MHz 2.7648Mbps	1.8432MHz 115.2Kbps	44.2368MHz 2.7648Mbps
External crystal 0.9216MHz		1.8432MHz 115.2Kbps		1.8432MHz 115.2Kbps
Other external frequency	Consult the dual UART mode table			

4. Register

The basic declare about register, PCI configuration spare, the bit explanation about configuration register can consult the first DataSheet.

4.1. Parallel port register

The parallel in CH352 compatible with SPP standard printer port and has enhanced, gray in the following table of register bit are enhanced functions. The actual address of parallel is I/O base address 1 adds the offset address in the table. The parallel in CH352 has four modes: SPP (contain Nibble, Byte and PS/2), EPP, ECP and 8255, the ALL in the table indicates all modes, ADV indicates EPP, ECP and 8255, PRT indicates SPP, EPP and ECP, RO indicates register read only, WO indicates register write only, R/W indicates register read and write.

Add.	Mode	R/W	Name	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
0	SPP	RO	PIR	D7IN	D6IN	D5IN	D4IN	D3IN	D2IN	D1IN	D0IN
0	ADV	RO	PIR	IBD7	IBD6	IBD5	IBD4	IBD3	IBD2	IBD1	IBD0
0	ALL	WO	PDR	D7OUT	D6OUT	D5OUT	D4OUT	D3OUT	D2OUT	D1OUT	D0OUT
1	8255	RO	PSR	!ACK#	INTR#	STB#	MCS1	MCS#	!INTFLAG	1	1
1	SPP	RO	PSR	!BUSY	ACK	PE	SELT	ERR		1	1
1	EPP	RO	PSR						1	1	!EPPREQ
1	ECP	RO	PSR						!ECPICMD	!ECPIBF	!ECPOUT
2	PRT	R/W	PCR	1	1	DIRIN	INTEN	!SIN	INIT	!AFD	!STB
2	8255	R/W	PCR	!8255OBF	1	8255IBF		GPO1	GPO0	0	0
3	SPP	R/W	PXR	0	0	0	0	0	0	0	0
3	EPP	R/W	PXR	0	0	0	0	EPPADDR	MODEEPP	0	0
3	ECP	R/W	PXR	0	0	0	ECPINTF	0	0	ECPDIRIN	MODEECP
3	8255	R/W	PXR	EN8255	MODE8255	0	0	0	0	0	0

The following are register default value after power-on reset or PCI bus reset.

Register name	Bit-7	Bit-6	Bit-5	Bit-4	Bit-3	Bit-2	Bit-1	Bit-0
PIR	1	1	1	1	1	1	1	1
PDR	0	0	0	0	0	0	0	0
PSR	!BUSY	ACK	PE	SELT	ERR	1	1	1
PCR	1	1	0	0	0	0	0	0
PXR	0	0	0	0	0	0	0	0
Others	Un-defined							

PIR: Data input register, input real time data from D7-D0 in SPP mode, and in EPP, ECP or 8255 mode, it is

input/upload buffer data which has latched. In EPP mode, the data is latched when AFD pin or SIN pin output low-level; and in ECP mode, the data is latched when ACK pin is low-level, and latch !ECPICMD at the same time; in 8255 mode, the data is written by external MCU when MCS1, MCS# and STB# are all valid then latched.

PDR: Data output register, used to write data which is ready to output/download. In SPP mode, data written to this register will output to D7-D0 pins. In EPP or ECP mode, write to this register will automatically execute data output or input handshake protocol; in 8255 mode, write to this register will set !8255OBF token and the OBF# pin is valid.

PSR: Status register, used to query input pin and operation execute status.

!BUSY: the opposite value of BUSY in SPP, EPP and ECP mode, when BUSY input high-level, this bit is 0.

ACK: ACK status in SPP, EPP and ECP mode.

PE: PE status in SPP, EPP and ECP mode.

SELT: SELT status in SPP, EPP and ECP

ERR: ERR status in SPP, EPP and ECP

!INTFLAG: the opposite value of interrupt token in SPP mode, when ACK is rising edge, this bit can be clear automatically, set as 1 after read PSR register.

!EPPREQ: the opposite value of storing operation token in EPP mode. When writing to PDR register, this bit can be clear automatically, and try EPP store transaction, the bit set as 1 until the operation is finished.

!ECPICMD: the opposite value of reverse transfer command in ECP mode, when reverse transfer is command, this bit is 0.

!ECPIBF: the opposite value of upload buffer full token in ECP mode reverse transfer, when upload buffer is full, the bit automatically clear as 0, and set as 1 after reading PIR register.

!ECPOUT: the opposite value of positive transfer transaction token in ECP mode. When write to PDR register, the bit automatically clear as 0, and try ECP positive direction transfer, the bit is set as 1 until operation is finished.

!ACK#: the opposite value of ACK# pin in 8255 mode, when ACK# input high-level, this bit is 0.

INTR#: INTR# state in 8255 mode.

STB#: STB# state in 8255 mode.

MCS1: MCS1 state in 8255 mode.

MCS#: MCS# state in 8255 mode.

PCR: control register, used to control output pins and transfer direction, interrupt enable.

DIRIN: bi-directional data wire D7-D0 tri-status output control in SPP, EPP and ECP mode. 0 indicates D7-D0 pin allowing tri-status output, 1 indicates D7-D0 forbid tri-status output.

INTEN: this bit is PCI interrupt output enable, 1 indicates allowing output interrupt query, 0 indicates forbidding output interrupt query.

!SIN: this bit is 1, SIN pin output valid (low active), or the SIN pin output invalid.

INIT: this bit is 1, INIT pin output invalid, or INIT pin output valid (low active).

!AFD: this bit is 1, AFD pin output valid (low active), or AFD pin output invalid.

!STB: this bit is 1, STB pin output valid (low active), or STB output invalid.

!8255OBF: the opposite value of output buffer is full in 8255 mode. When write to PDR register, this bit automatically clear as 0. Until MCS1, MCS# and ACK# id valid, and the data is taken by the external MCU, the bit is set as 1.

8255IBF: input buffer is full token in 8255 mode. When MCS1, MCS# and STB# are all valid, and the external MCU write data, the bit automatically set as 1; after read PIR register, the bit automatically clear as 0.

GPO1: this bit is 1, GPO1 output valid (low active), or GPO1 output invalid.

GPO0: this bit is 1, GPO0 output invalid, or GPO0 output valid (low active).

PXR: configure register, used to set parallel work mode.

EPPADDR: target space select in EPP mode, 1 indicates address store transaction in EPP, 0 indicates data store transaction.

MODEEPP: when this bit is 1, use EPP mode.

ECPINTF: interrupt token in ECP mode, when ERR falling edge generate interrupt token, this bit is set as 1, set as 0 after read PXR register.

ECPDIRIN: transfer direction control in ECP mode, 0 indicates ECP positive transfer/output, 1 indicates ECP reverse transfer/input.

MODEECP: when this bit is 1, use ECP mode.

MODE8255: when this bit is 1, use 8255 mode, then EN8255 is 1, this bit can be modify, or keep the former value.

EN8255: when this bit is 1, MODE8255 can be modify, or the MODE8255 keep the former value, and return 0 when read this bit.

5. Function

5.1. Query and interrupt

The UART and parallel share one PCI interrupt query pin in CH352. After entering PCI interrupt service, analyse whether it is CH352 query interrupt, and which serial or parallel is interrupting. When entering interrupt service, read PSR and PXR register in parallel. If it is ECP mode, check ECPINTF token in PXR register, or check !INTFLAG token in PSR register. If it is valid, indicates there is interrupt, deal with it and then quit; if it is invalid, indicates there is no interrupt, read the IIR register in serial-0, if there is interrupt, deal with it then quit; there is no interrupt then quit directly.

If serial works on interrupt mode, set IER register to allow relative interrupt query, and set OUT2 in MCR register to allow output interrupt.

If parallel works on interrupt mode, set INTEN in PCR register to allow output interrupt. In SPP or EPP mode, starting interrupt query with ACK rising edge. In ECP mode, starting interrupt query with ERR falling edge. In 8255 mode, starting interrupt query with INTR# rising edge.

If serial works on query mode, un-set IER and MCR, query LSR register and deal with it.

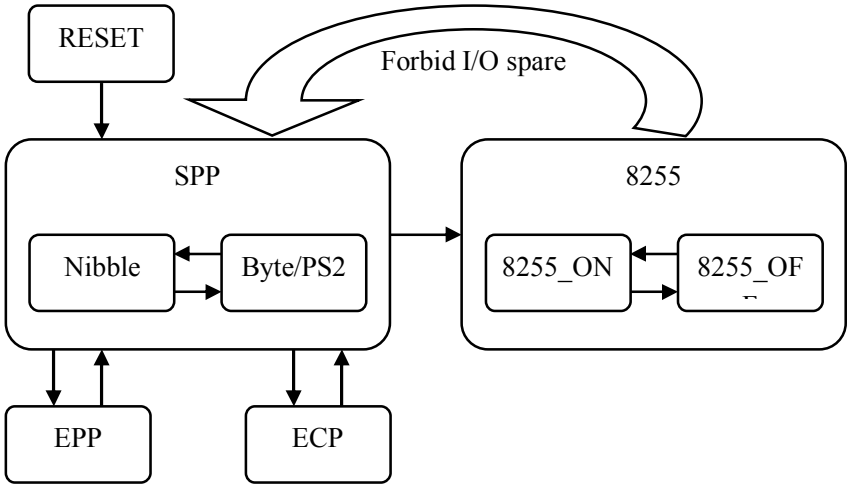
If parallel works on query mode, un-set INTEN in PCR, query PSR, PCR and PXR register and deal with it.

5.2. Serial transaction

The detail information can consult CH352DS1.PDF or serial chip 16C550 or dual UART CH432.

5.3. Parallel transaction

The three modes of parallel in CH352 can not coexist, SPP is in default. Realize Nibble, Byte and PS/2 etc. mode in SPP mode. Set PXR register to realize switch between SPP, EPP or ECP. But 8255 is an special mode which can be locked by itself. After set PXR register to enter into 8255 mode, it can not switch to SPP, EPP or ECP mode, unless the bit-0 in command register of PCI configuration spare is set as 0 (forbid I/O spare) or PCI bus reset. Or only select between open 8255 or close 8255. The following is switch table of parallel.



In SPP mode, use software to control PCR and query PSR to realize Nibble, Byte and PS/2 etc. transfer, the detail information can consult IEEE1284 criterion.

In 8255 mode, the parallel in CH352 is similar with industrial standard 8255 chip mode 2, support hardware handshake signal and chip select input, bi-directional data transfer, can be connected with the data bus of external MCU. For download, write data to PDR, then query PSR until !8255OBF is 1; for upload, query PSR until 8255IBF is 1, then read data from PIR (read with PSR to enhance the efficiency). For interrupt application, computer can set GPO0 or GPO1 to notify the interrupt to MCU before download. And the MCU also can set INTR# to notify interrupt to computer before upload. The following table is operation about first query and then store. Chip select is valid means MCS1 is high level and MCS# is low level, it can be drove by chip select encode circuit in MCU, or drove by two address wires in MCU. ACK# is drove by read control signal RD in MCU, STB# is drove by write control signal WR in MCU.

Direction	Computer endpoint, CH352 endpoint	Peripheral device endpoint, MCU endpoint	Explanation
download	Wait !8255OBF is 1 in PCR	Query OBF# state	Wait the former to finish
	Write download data to PDR		OBF# output low-level
		Check OBF# is valid（low-level）	
		Chip select valid and ACK# is low-level, get data out	OBF# output high
	(!8255OBF automatic set as 1 in PCR)		download finish
upload	Query 8255IBF token in PCR	Wait IBF invalid (low-level)	Wait the former to finish
		Chip select valid and STB# is low-level, write data	IBF output high
	Check 8255IBF in PCR is 1		
	Read the upload data from PIR		IBF output low-level
		（IBF auto invalid）	upload finish

5.4. Application

The application about UART can consult the first datasheet.

In order to work, the serial of CH352 needs the external to provide clock signal for XI. Generally, clock signal is generated by inverter in CH352 through oscillating of crystal keeping frequency. If the UART

function doesn't need, the XI doesn't need clock; get out of the crystal and oscillating capacitance, XI must connect to ground directly.

The parallel output pins are CMOS level in CH352, compatible with TTL level. The input pins are compatible with CMOS level and TTL level, and the input pins have set with pull-up resistor which is necessary for printer ports. So the peripheral circuit is simplified.

In UART, CH352 contains these pins: bi-direction data pin, control output pin and state input pin. Except INIT, the bi-direction data pin and control output pin are high-level in default. In SPP mode, all the pins can be used as common IO pin, controlled and defined function by computer application program.

In Windows and Linux OS, the drive of CH352 is compatible with standard printer port, so the most former parallel application programs are compatible, no need to modify.

CH352 can be used to expand the extra high speed RS232 serial and parallel/printer port, and PCI card of internal embedded MCU to deal with data

6. Parameter

6.1. Absolute maximum rating (Stresses above those listed can cause permanent damage to the device. Exposure to maximum rated conditions can affect device operation and reliability.)

Name	Parameter note		Min.	Max.	Units
TA	Operation temperature	VCC=5V	-40	85	℃
		VCC=3.3V	-40	65	
TS	Storage temperature		-55	125	℃
VCC	Source Voltage（VCC connects to power, GND connects to ground）		-0.5	6.0	V
VIO	Voltage at input or output pin		-0.5	VCC+0.5	V

6.2. Electrical parameter (test conditions: TA=25℃,VCC=5V,exclude pin connection of PCI bus)

(The every current parameter must multiply the coefficient of 40% when the power is 3.3V)

Name	Parameter note	Min.	Typical	Max.	Units
VCC	Supply voltage（consult the following note）	3.3	5	5.3	V
ICC	Operate current	1	15	50	mA
VIL	Input voltage (LOW)	-0.5		0.8	V
VIH	Input voltage(HIGH)	2.0		VCC+0.5	V
VOL	Output voltage LOW（4mA draw current）			0.5	V
VOH	Output voltage HIGH（2mA output current）	VCC-0.5			V
IIN	Input current at input pin without pull-up resistor			10	uA
IUP1	Input current at input pin with feeble pull-up resistor	3	5	170	uA
IUP2	Input current at input pin with pull-up resistor	180	250	500	uA
IUP3	Input current in input pin with strong pull-up resistor	220	350	800	uA
IUPscl	Pull-up input current in SCL pin	150	250	400	uA
IDN	Input current in input pin with pull-down resistor	-18	-30	-80	uA

Note: The input endurance voltage is source voltage adds 0.5V of CH352. For example, when CH352 works in 3.3V, the outside providing voltage can't pass 3.8V. When the source voltage of CH352 is lower than 4V, the host frequency of PCI bus is no pass 33MHz, as PCI bus can't work at above 33MHz.

6.3. Time sequence parameter (test conditions: TA=25℃, VCC=5V, FCLK=33.3MHz)

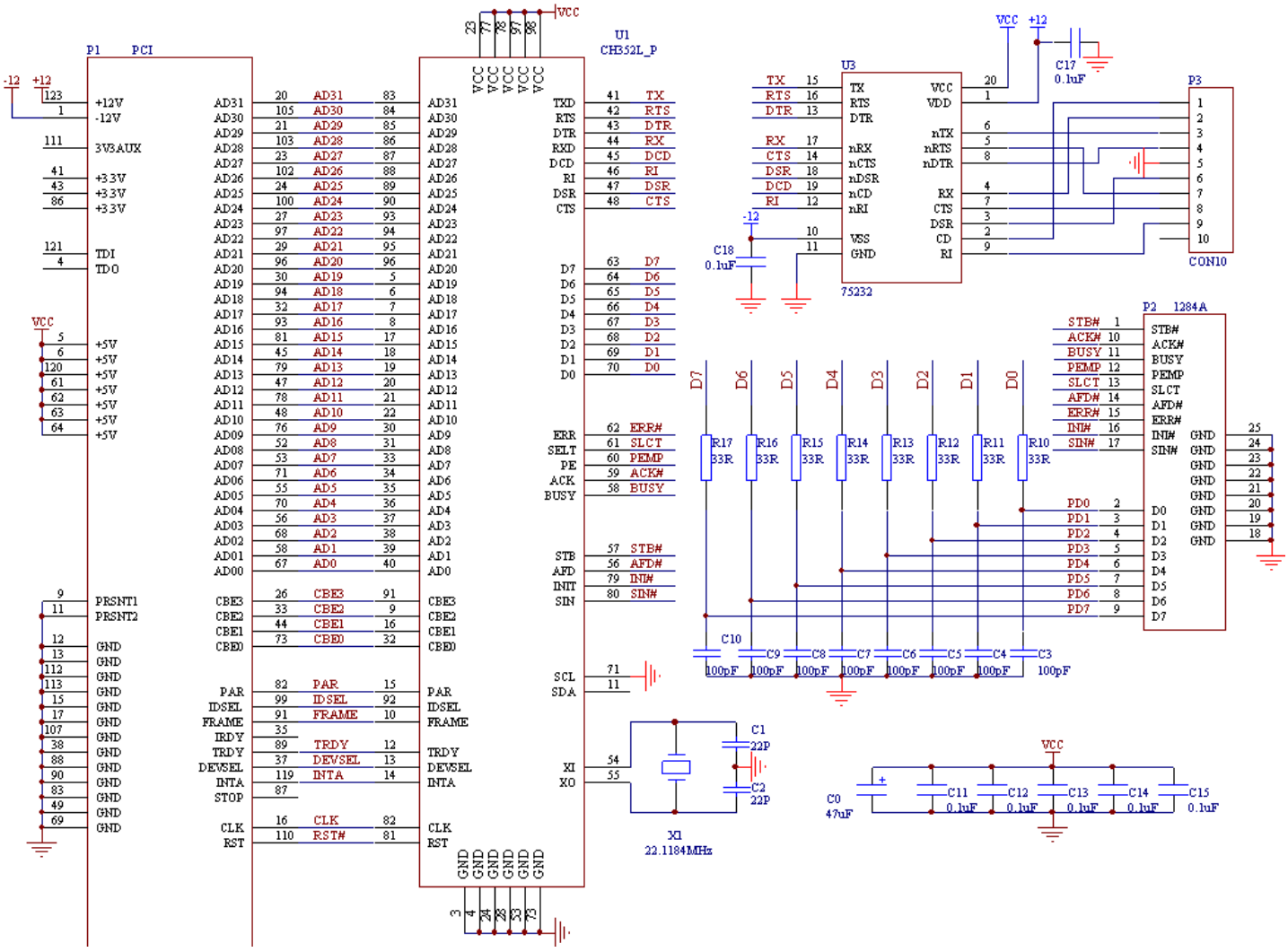
Name	Parameter note	Min.	Typical	Max.	Units
FCLK	CLK input frequency（PCI bus host frequency）	0	33.3	40	MHz
FSCL	SCL output frequency when auto load（2-wire interface host frequency）	FCLK / 128 = 260			KHz
FXI	XI input frequency, crystal frequency	0.9216	22.1184	32	MHz
TWSTB	STB# valid low-level width in 8255 mode	40			nS
TWACK	ACK# valid low-level width in 8255 mode	40			nS
TDOON	ACK# valid to data output valid in 8255 mode	0		20	nS
TDOOF	ACK# invalid to data output invalid in 8255 mode	0		30	nS

7. Application

7.1. UART + printer port (following image)

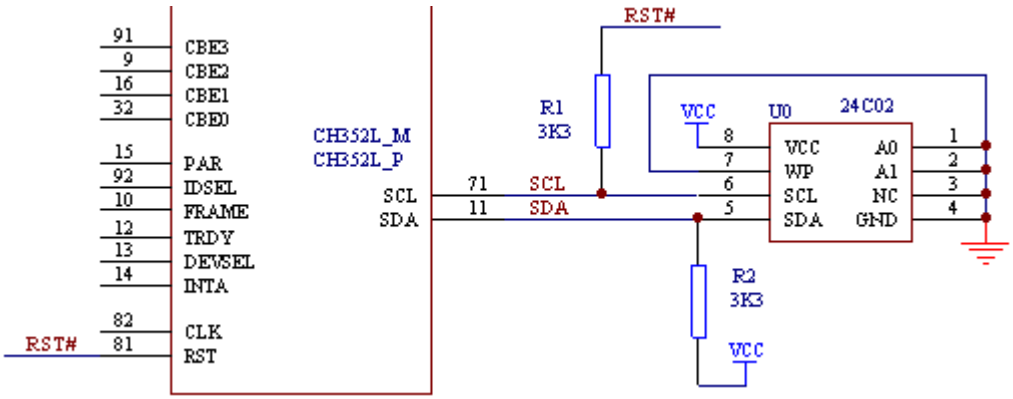
This is UART + printer port / parallel circuit based on CH352 chip. U3 is RS232 level convert chip 75232, P3 is 10 pins two lines needles or DB9 needles. P2 is IEEE1284 type A DB25 needle (printer port connection). Serial connection resistor R10~R17 and parallel connection capacitance C3~C10 are used to parallel data wire impedance matching, they can be ignored.X1, C1 and C2 are used for clock oscillator circuit. C0, C11~C15 and C17~C18 are used to power decoupling. C11~C15 and C17~C18 are 0.1uF capacitances, they are made of monolithic or high frequency ceramic, connect next to three power pins in CH352 or 75232 chip.

CH352 is high frequency numeric circuit, pay attention on signal impedance matching, consult PCI criterion when designing PCB board. The PCI signal wire is less than 35mm in CH352, adapt arc wire or 45 degree wire, avoid right-angle or acute angle wire. Lay the signal wire in elements side, spare the other side to connect with ground. The length of CLK is between 50mm~65mm, it isn't near with other signal wire. Recommend to connect with ground or cover copper beside CLK and or the other side PCB board, decrease the disturber by other signal wires.



7.2. Connect configuration chip (following image)

The following is CH352 connect with external configuration chip 24C02 in UART+parallel mode, R2 is used to SDA pull up. SCL via R1 connect to RST pin of PCI global reset pin, not connect to ground.



7.3. Connect MCU (following image)

PC via CH3352 to bi-direction transfer data with MCU or DSP, there are three methods: the first is using UART to communication; the second is ECP parallel mode which support automatic hardware handshake; the third is using 8255 parallel mode, CH352 directly connect to data bus of MCU, and it is as common peripheral device to store.

The following circuit is about MCS51 MCU 89C51 via data bus connect with CH352 which is working on 8255 mode. Using address encode U3 to generate chip select MCS# in CH352. If the MCU peripheral device is very few, the U3 can be ignored, use P27 to directly drive MCS1 in CH352, P26 drive MCS#. For MCU, this connection, the address of CH352 is 0B000H, when MCU checks 0BF# is valid, read 0B000H address, get the download data and auto invalid 0BF#; when MCU checks IBF invalid, if need to upload, write upload data to address 0B000H and auto valid IBF, until PC get the upload data and auto invalid IBF.