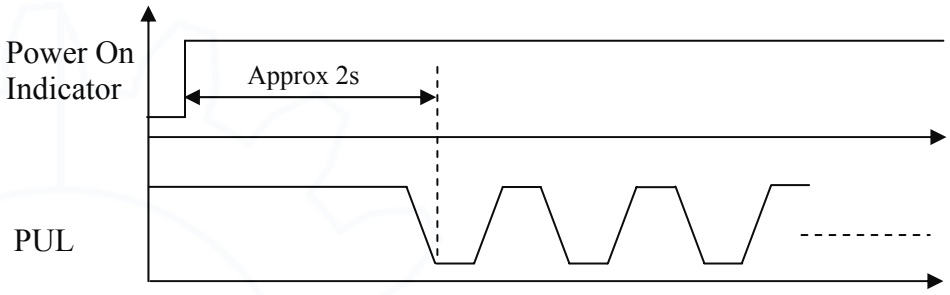
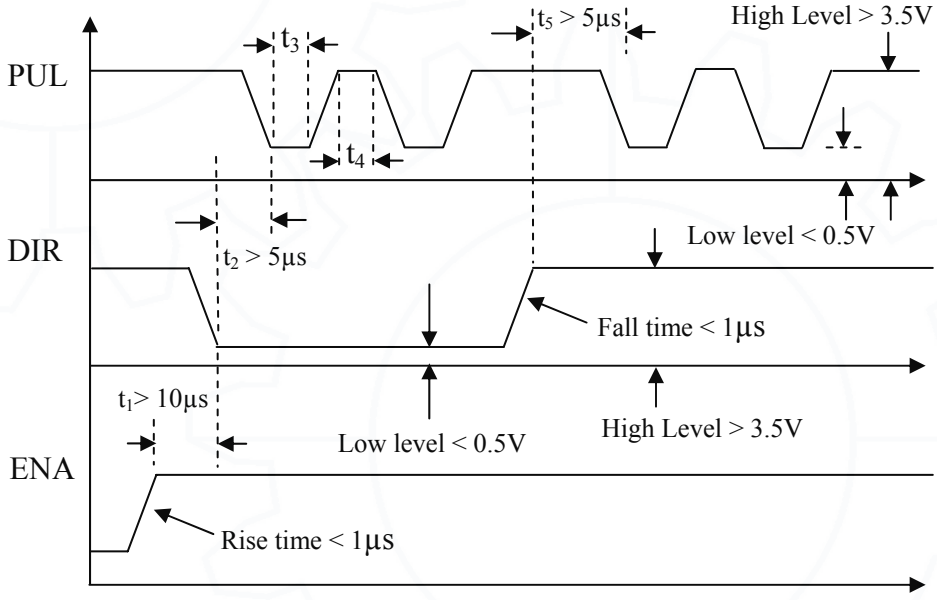
Signals Timing Sequence

In order to avoid some operation problem, fault and deviation of performance, the Pulse (PUL), Direction (DIR) and Enable (ENA) must abide to the criteria, as shown in the diagram below:



Power On Sequence Timing Chart

The power on period varies on the input AC voltage. Typical power on period is 2 seconds when for +48VDC.



Control Signal Sequence Timing Chart

Remarks:

1) ENA (must be ahead of DIR by at least 10µs, (t_1) logic HIGH as valid. Generally ENA+ and ENA- is NC (not connected)

(2) DIR must be ahead of PUL effective falling edge by 5µs to ensure correct direction (t_2 & t_5).

(3) Low and High level Pulse width not less than 2µs (t_3 & t_4)

(4) Rise and Fall time of all signal must be less than 1µs